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K4C11 K5E4

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(54) Abstract Title

Method of fabricating a dynamic random access memory device

(57) A titanium layer 62 is formed between the top electrode 61 of the capacitor of the DRAM and the interlevel dielectric layer 63 to reduce the stress and enhance adhesion therebetween. A titanium oxide layer and a titanium nitride layer are formed between the titanium layer 62 and the interlevel dielectric layer 63 in post deposition thermal procedures, which enhances adhesion and avoids cracks which allow leakage current between the top electrode and the interlevel dielectric layer 63. The top electrode 61 may be tungsten, platinum, ruthenium, tungsten nitride, molybdenum, molybdenum nitride or tantalum. The interlevel dielectric 63 may be BPSG or PSG. The capacitor dielectric 60 may be barium strontium titanate, lead zinc titanate or tantalum oxide.

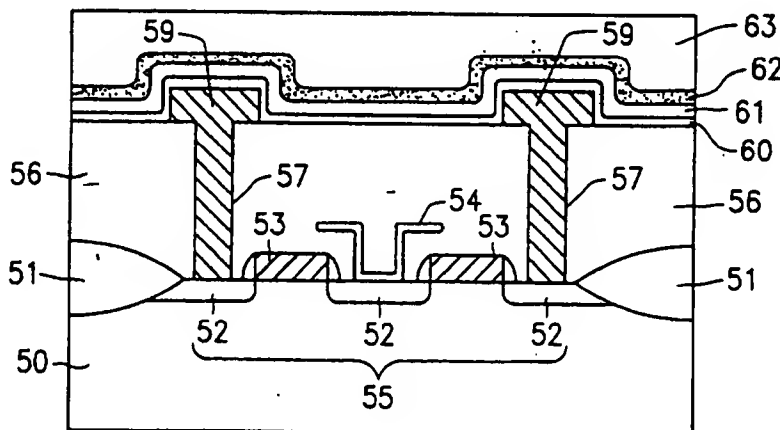


FIG. 3C

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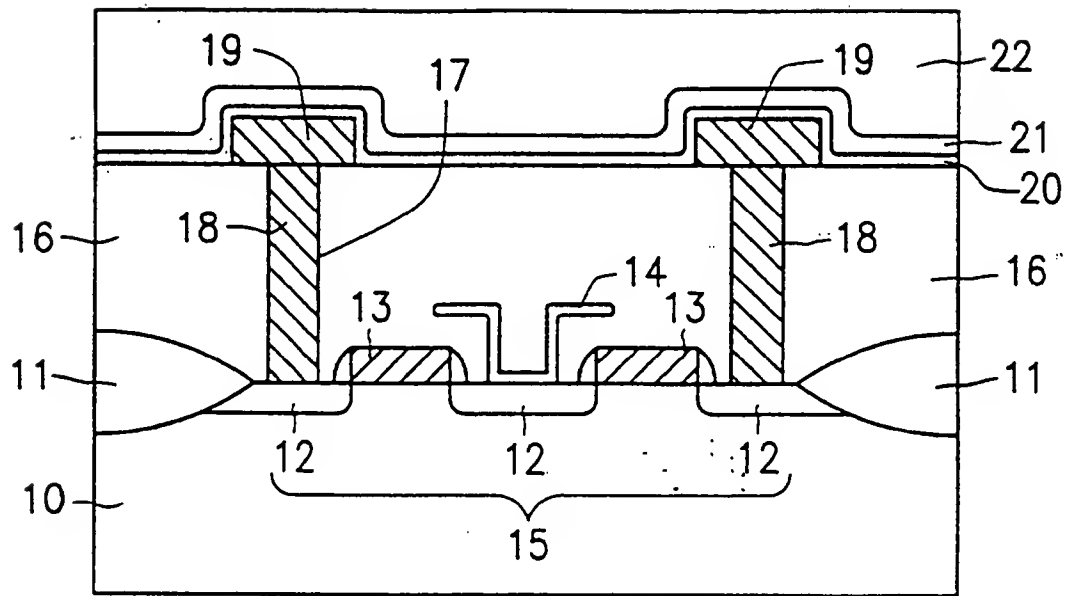


FIG. 1 (PRIOR ART)

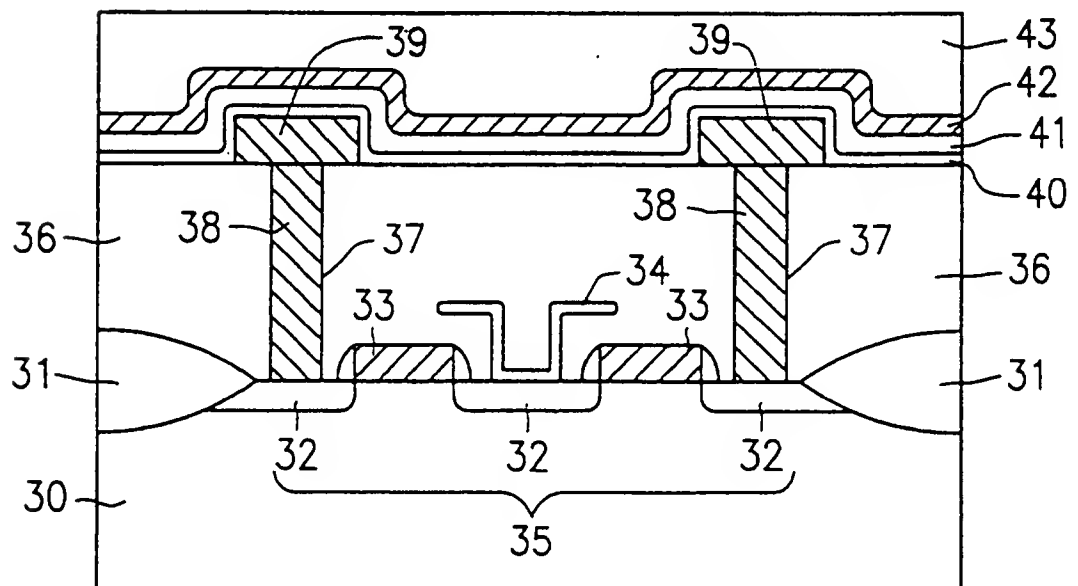


FIG. 2 (PRIOR ART)

A cross-sectional view of a semiconductor device. The device features a central channel region (54) flanked by two side gate regions (57). The channel region is defined by a central gate (53) and is surrounded by a gate oxide layer (52). The side gate regions are also defined by gate oxide layers (52) and are separated from the channel region by a gate oxide layer (52). The device is mounted on a substrate (50) and is covered by a passivation layer (51). The top surface of the device is covered by a passivation layer (56). The device is connected to a power supply (59) and a ground (60).

FIG. 3B

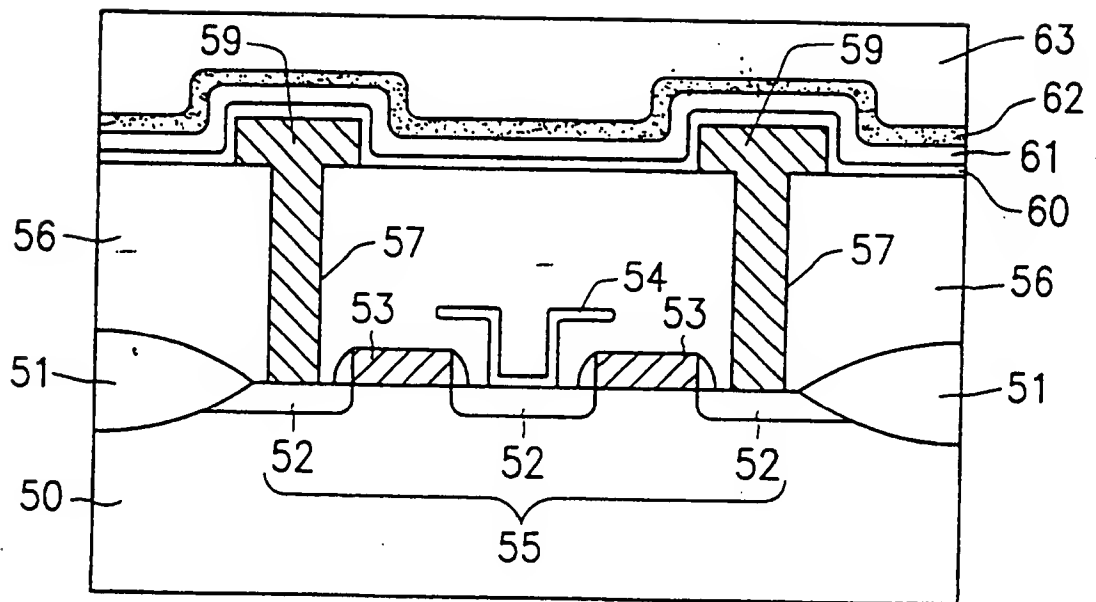


FIG. 3C

METHOD OF FABRICATING A DYNAMIC RANDOM ACCESS MEMORY
DEVICE

BACKGROUND OF THE INVENTION

5

Field of the Invention

This invention relates to a method of fabricating a dynamic random access memory (DRAM) device, and more particularly to a method of fabricating a DRAM device for reducing the stress between a top electrode of a DRAM capacitor and an
10 interlevel dielectric layer.

Description of Related Art

The main purpose of the capacitor in a DRAM device is to save logical data. The capacity in a DRAM device must be large enough, so the data access time can be faster.
15 When the device size scales down, the capacity decreases. It is typical to use a high-k dielectric material for DRAM capacitors. Using the high-k dielectric can increase the capacity in the same thickness of dielectric.

The semiconductor structure configuration of a high-k dielectric material for a conventional DRAM device memory cell unit is shown in the cross-sectional schematic
20 view in FIG. 1. A field oxide layer 11, polygate layer 13, source/drain regions 12 and word line 14 of a MOS transistor 15 are formed over the surface of a silicon substrate 10. After the formation of the transistor 15, an oxide layer 16 is deposited over the surface of the substrate 10. Contact openings 17 are formed at designed locations above the source/drain regions 12 by etching. The contact openings 17 are then filled with a

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conductive material, such as tungsten, to form plugs 18. A conductive layer 19, such as a heavily doped polysilicon layer, is deposited over the plugs 18 to form a bottom electrode of the capacitor. A dielectric layer 20, such as a tantalum oxide (Ta_2O_5) layer, is deposited on the top of the conductive layer 19 and oxide layer 16. A titanium nitride layer 21 is deposited over the dielectric layer 20 to form a top electrode of the capacitor. Then, an interlevel dielectric layer 22, such as a borophosphosilicon glass (BPSG) layer, is formed over the titanium nitride layer 21 to complete the fabrication of the conventional DRAM device.

The titanium nitride layer 21 is used as the top electrode of the DRAM capacitor, while the dielectric layer is a high-k dielectric layer in the above DRAM device. The stress between titanium nitride layer 21 and interlevel dielectric layer 22 of the DRAM capacitor will increase when the temperature is above 600°C . This will cause interlevel dielectric layer 22 to crack, thus increasing leakage current during the following BPSG reflow for planarization.

Thus, to reduce the stress between titanium nitride layer 21 and interlevel dielectric layer 22 and to decrease the crack and the leakage current, a polysilicon layer is formed between the titanium nitride layer 21 and the interlevel dielectric layer 22 to overcome the above problems. Another semiconductor structure configuration of a high-k dielectric material for a conventional DRAM device memory cell unit is shown in the cross-sectional schematic view in FIG. 2. A field oxide layer 31, polygate layer 33, source/drain regions 32 and word line 34 of the MOS transistor 35 are formed over the surface of a silicon substrate 30. After the formation of the transistor 35, an oxide layer 36 is deposited over the surface of the substrate 30. Contact openings 37 are formed at designed locations above the source/drain regions 32 by etching. The contact openings

37 are then filled with a conductive material, such as tungsten, to form plugs 38. A conductive layer 39, such as a heavily doped polysilicon layer, is deposited over the plugs 38, and forms a bottom electrode of the capacitor. A dielectric layer 40, such as a tantalum oxide layer, is deposited on the top of the conductive layer 39 and oxide layer 36. A titanium nitride layer 41 is deposited over the dielectric layer 40 to form a top electrode of the capacitor. Then, a polysilicon layer 42 is deposited over the titanium nitride layer 41. An interlevel dielectric layer 43, such as a borophosphosilicon glass layer, is formed over the titanium nitride layer 41 to complete the fabrication of this conventional DRAM device.

10 The known methods to form a polysilicon layer between the titanium nitride layer and the interlevel dielectric layer make the fabrication more complex and expensive, though it does reduce crack formation and leakage current.

SUMMARY OF THE INVENTION

15 It is therefore an object of the present invention to provide a method of fabricating a DRAM device which avoids crack formations and leakage current between the top electrode and the interlevel dielectric layer, by forming a titanium layer between the top electrode and the interlevel dielectric layer.

20 It is another object of the present invention to provide a method of fabricating the DRAM device, which reduces the stress and enhances the adhesion between the top electrode and the interlevel dielectric layer, by forming a titanium layer between the top electrode and the interlevel dielectric layer.

 It is a further object of the present invention to provide a method of fabricating the DRAM device, in which the titanium layer and titanium nitride layer are formed in

the same chamber. This reduces the complexity of fabricating the DRAM device and the costs.

The method of fabricating the DRAM device includes: forming a transistor including a gate, a source/drain region and a word line on a silicon substrate. An oxide layer is formed covering the transistor. A contact opening is formed in the oxide layer to expose the surface of the source/drain region. A conductive layer is formed in the contact opening and covering the oxide layer. The conductive layer is patterned to form a plurality of bottom electrodes. The bottom electrodes are coupled with the source/drain region by the contact opening. A dielectric layer is formed over the surface of the bottom electrodes and the oxide layer. A top electrode is formed covering the high-k dielectric layer. A titanium layer is formed on the top electrode. Then, an interlevel dielectric layer is formed on the titanium layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features, and advantages of the present invention will become apparent by way of the following detailed description of the preferred but non-limiting embodiment. The description is made with reference to the accompanying drawings in which:

Figure 1 is a cross-sectional view showing a conventional memory cell unit for a DRAM device;

Figure 2 is a cross-sectional view showing another conventional memory cell unit for a DRAM device; and

Figures 3A-3C show cross-section views of a memory cell unit for a DRAM device fabricated in accordance with a preferred embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A detailed description of the process of the invention follows with reference to Figs. 3A-3C, which show the cross-section of a memory cell unit of a DRAM device fabricated in accordance with this invention. Note that these schematic drawings are not presented to the exact physical dimensional scale, as they serve the major purpose of illustrating the process steps of the invention.

Referring to FIG. 3A, a silicon substrate 50 is provided as the basis for the construction of the DRAM device. A field oxide layer 51, polysilicon gate layer 53, source/drain regions 52, and word line 54 of the MOS transistor 55 are formed over the surface of the silicon substrate 50. Then, a chemical vapor deposition procedure, for example, is used to form an oxide layer 56 on the top of the MOS transistor 55. The oxide layer 56 is patterned to form a contact opening 57 over the source/drain regions 52. A conductive layer 58 is deposited over the oxide layer 56 and the contact opening 57. The conductive layer 58 is filled in the contact opening 57. The conductive layer 58 can be, for example, a heavily doped polysilicon layer, a hemispherical grain polysilicon, tungsten, platinum, ruthenium, tungsten nitride, titanium nitride, molybdenum, molybdenum nitride or tantalum nitride.

Referring to FIG. 3B, the conductive layer 58 is patterned to form a plurality of bottom electrodes 59 coupled with the source/drain regions 52 by way of the contact opening 57. A high-k dielectric layer 60, such as a barium strontium titanate, lead zinc titanate or tantalum oxide layer, is deposited over the bottom electrodes 59 and the exposed oxide layer 56. Then, a top electrode 61 is formed on the surface of the high-k dielectric layer 60. The top electrode 61, for example, can be a tungsten, platinum,

ruthenium, tungsten nitride, titanium nitride, molybdenum, molybdenum nitride or tantalum nitride layer.

Referring to FIG. 3C, a chemical vapor deposition or a physical vapor deposition procedure, for example, is utilized to deposit a titanium layer 62 on the top of the top electrode 61. The titanium layer 62 and the titanium nitride layer can be formed in the same chamber. Thus, the fabricating cost is reduced. Finally, an interlevel dielectric layer 63, such as a borophosphosilicon glass or phosphosilicon glass layer, is formed over the titanium layer 62. Since the post fabrication steps are not relevant in the context of the invention, they are not elaborated on here.

Resultantly, the stress between the titanium layer 62 and the interlevel dielectric layer 63 is smaller, so that to form the titanium layer 62 between the top electrode layer 61, such as a titanium nitride layer, and the interlevel dielectric layer 63 reduces the stress between the top electrode layer 61 and the interlevel dielectric layer 63. In addition, a titanium oxide layer and a titanium silicide layer are formed between the titanium layer 62 and the interlevel dielectric layer 63 in post thermal procedures. This enhances the adhesion and avoids crack formation and leakage current.

While the invention has been described by way of example and in terms of a preferred embodiment, it is to be understood that the invention need not be limited to the disclosed embodiment. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structures.

WHAT IS CLAIMED IS:

1. A method of fabricating a DRAM device, comprising:
forming a transistor including a gate, a source/drain region and a word line on a silicon substrate;
5 covering the transistor with an oxide layer;
forming a contact opening in the oxide layer to expose a surface of the source/drain region;
forming a conductive layer in the contact opening and covering the oxide layer;
patterning the conductive layer to form at least one bottom electrode which is coupled
10 with the source/drain region by way of the contact opening;
forming a dielectric layer over a surface of the bottom electrode and the oxide layer;
covering the dielectric layer with a top electrode;
forming a titanium layer on the top electrode; and
forming an interlevel dielectric layer on the titanium layer.
15
2. The method according to claim 1, wherein said covering the transistor includes forming the oxide layer using chemical vapor deposition.
3. The method according to claim 1, wherein said forming a conductive layer includes
20 forming the conductive layer from a material selected from the group consisting of a heavily doped polysilicon, a hemispherical grain polysilicon, tungsten, platinum, ruthenium, tungsten nitride, titanium nitride, molybdenum, molybdenum nitride and tantalum nitride layer.

4. The method according to claim 1, wherein said forming a dielectric layer includes forming a high-k dielectric layer.

5. The method according to claim 4, wherein the high-k dielectric layer is selected from the group consisting of barium strontium titanate, lead zinc titanate and tantalum oxide.

6. The method according to claim 1, wherein said covering the dielectric layer includes forming the top electrode from a material selected from the group consisting of tungsten, platinum, ruthenium, tungsten nitride, titanium nitride, molybdenum, molybdenum nitride and tantalum nitride.

7. The method according to claim 1, wherein said forming an capacitor electrode and titanium layer includes using chemical vapor deposition.

8. The method according to claim 1, wherein said forming an capacitor electrodes and titanium layer includes using physical vapor deposition.

9. The method according to claim 1, wherein said forming an interlevel dielectric layer includes forming an interlevel dielectric borophosphosilicon glass layer.

10. The method according to claim 1, wherein said forming an interlevel dielectric layer includes forming an interlevel dielectric phosphosilicon glass layer.

11. The method according to claim 1, wherein said patterning includes forming a plurality of bottom electrodes, each being coupled to a respective source/drain region.

12. A method of fabricating a DRAM device, comprising:

- 5 forming a dielectric layer over a surface of a bottom electrode and an oxide layer;
 covering the dielectric layer with a top electrode;
 forming a titanium layer on the top electrode; and
 forming an interlevel dielectric layer on the titanium layer.

13. A method of fabricating a DRAM device, substantially as hereinbefore described with reference to and/or as illustrated in any one of or any combination of Figures 3A-C of the accompanying drawings.

Amendments to the claims have been filed as follows

CLAIMS

1. A method of fabricating a DRAM device, comprising:

forming a transistor including a gate, a source/drain region and a word line on a silicon substrate;

covering the transistor with an oxide layer;

forming a contact opening in the oxide layer to expose a surface of the source/drain region;

forming a conductive layer in the contact opening and covering the oxide layer;

patterning the conductive layer to form at least one bottom electrode which is coupled with the source/drain region by way of the contact opening;

forming a dielectric layer over a surface of the or each bottom electrode and the oxide layer;

covering the dielectric layer with a titanium nitride layer to form a top electrode;

forming a titanium layer on the top electrode; and

forming an interlevel dielectric layer.
2. The method according to claim 1, wherein said covering the transistor includes forming the oxide layer using chemical vapour deposition.
3. The method according to claim 1, wherein said forming a conductive layer includes forming the conductive layer from a material selected from the group consisting of a heavily doped polysilicon, a hemispherical grain polysilicon, tungsten, platinum, ruthenium, tungsten nitride, titanium nitride, molybdenum nitride and a tantalum nitride layer.

4. The method according to claim 1, wherein said forming a dielectric layer includes forming a high-k dielectric layer.
5. The method according to claim 4, wherein the high-k dielectric layer is selected from the group consisting of barium strontium titanate and tantalum oxide.
6. The method according to claim 1, wherein said forming a top electrode and titanium layer includes using chemical vapour deposition.
7. The method according to claim 1, wherein said forming a top electrode and titanium layer includes using physical vapour deposition.
8. The method according to claim 1, wherein said forming an interlevel dielectric layer includes forming an interlevel dielectric borophosphosilicon glass layer.
9. The method according to claim 1, wherein said forming an interlevel dielectric layer includes forming an interlevel dielectric phosphosilicon glass layer.
10. The method according to claim 1, wherein said patterning includes forming a plurality of bottom electrodes, each being coupled to a respective source/drain region.

11. A method of fabricating a DRAM device, comprising:
 - forming a dielectric layer over a surface of a bottom electrode and an oxide layer;
 - covering the dielectric layer with a titanium nitride layer so as to form a top electrode;
 - forming a titanium layer on the top electrode;
 - forming an interlevel dielectric layer on the titanium layer; and
 - performing a reflow process to planarise the interlevel dielectric layer.
12. The method of claim 11, wherein said forming an interlevel dielectric layer includes forming an interlevel dielectric borophosphosilicon glass layer.
13. The method of claim 11, wherein said forming an interlevel dielectric layer includes forming an interlevel dielectric phosphosilicon glass layer.
14. A method of fabricating a DRAM device, substantially as hereinbefore described with reference to and/or as illustrated in any one or combination of figures 3A to C of the accompanying drawings.



Application No: GB 9727213.2
Claims searched: 1-13

Examiner: Miss E.L.Rendle
Date of search: 26 March 1998

**Patents Act 1977
Search Report under Section 17**

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H1K (KGAMS. KGAMX)

Int Cl (Ed.6): H01L 21/8242, 27/108

Other: Online: WPI, INSPEC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
X	US 5 670 808 (TOSHIBA) see whole document, especially figures 25a-d, figures 29a-d, column 1 lines 51-56, column 13 lines 7-55 and column 16 lines 17-49.	1-12.

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.